Listing of the Claims:

The following is a complete listing of all the claims in the application, with an indication of the status of each.

1. (Currently Amended) A data processing device including:

a processor;

a charge storage device coupled to the processor;

a current source for supplying the processor with substantially constant operating current at multiple nonzero current levels, and adapted to vary its output current independently of an instantaneous power demand of the processor by switching, on at least one of a periodic and an aperiodic basis, ~~either periodically or aperiodically~~ between the multiple nonzero current levels.

2. (Currently Amended) The device of claim 1 wherein ~~in which~~ the charge storage device comprises a capacitor in series with the current source, and across which the processor is connected in parallel.

3. (Currently Amended) The device of claim 1 wherein ~~in which~~ the current source is adapted ~~to periodically or aperiodically~~ switch between two different nonzero current levels.

4. (Canceled)

5. (Currently Amended) The device of claim 3 wherein ~~in which~~ the current source is adapted to determine the interval between switching current levels based on ~~is determined by~~ an average power demand of the processor.

6. (Currently Amended) The device of claim 1 wherein ~~in which~~ the current source further comprises:

a second current source adapted to provide a noise current, superposed on the substantially constant current, that varies on at least one from among a random and ~~or~~ pseudo-random basis.

7. (Currently Amended) The device of claim 1 further including a control means for controlling the current source ~~adapted~~ to maintain the supply voltage to the processor between an upper voltage limit and a lower voltage limit.

8. (Currently Amended) The device of claim 1 further including a zener diode connected to the processor ~~adapted~~ to maintain the supply voltage to the processor between an upper voltage limit and a lower voltage limit.

9. (Currently Amended) The device of claim 7 wherein ~~in which~~ the control means includes a current switching means for switching the current source between a first, higher current level and a second, lower current level, the

current level switching being triggered by the supply voltage to the processor respectively reaching the lower voltage limit and the upper voltage limit.

10. (Original) The device of claim 9 further including a timer for determining a time period taken for the processor supply voltage to reach a lower voltage limit from an upper voltage limit, or vice versa.

11. (Currently Amended) The device of claim 10 wherein the timer determines whether the time period falls outside predetermined limits, and further including current setting means for varying at least one from among the first current level and ~~and/or~~ the second current level of the current source if the timer determines that the time period falls outside the predetermined limits.

12. (Currently Amended) The device of claim 11 wherein the predetermined limits include a first predetermined threshold, and wherein ~~in which~~ the current setting means raises the first current level if the timer determines that the time period for reaching the lower voltage limit falls below the [[a]] first predetermined threshold.

13. (Currently Amended) The device of claim 11 wherein the predetermined limits include a second predetermined threshold, and wherein ~~in which~~ the current setting means reduces the first current level if the timer determines

that the time period for reaching the lower voltage limit exceeds the [[a]] second predetermined level.

14. (Currently Amended) The device of claim 11 wherein the predetermined limits include a first predetermined threshold, and wherein ~~in which~~ the current setting means reduces the second current level if the timer determines that the time period for reaching the upper voltage limit exceeds the [[a]] first predetermined level.

15. (Currently Amended) The device of claim 11 wherein the predetermined limits include a second predetermined threshold, and wherein ~~in which~~ the current setting means raises the second current level if the timer determines that the time period for reaching the upper voltage limit exceeds the [[a]] second predetermined level.

16. (Currently Amended) The device of claim 9 wherein ~~in which~~ the control means includes means for temporarily inhibiting the current switching means if the supply voltage to the processor fails to move towards the ~~desired~~ upper voltage limit or the lower voltage limit.

17. (Currently Amended) The device of claim 1 wherein ~~in which~~ the processor has an internal clock having a ~~, the~~ frequency that ~~of which~~ is dependent upon the supply voltage to the processor.

18. (Currently Amended) The device of claim 1 wherein ~~in which~~ the processor is a cryptographic processor.

19. (Currently Amended) The device of claim 1 further comprising a ~~incorporated into~~ a smart card supporting the processor, the charge storage device, and the current source.

20. (Currently Amended) A method of operating a data processing device having a processor and a charge storage device connected to the processor, comprising ~~the steps of~~:

providing a current source drawing current from an external power supply; and

~~utilizing the drawn current to~~ cyclically apportioning a substantially constant current flow from current source between a charge storage device and the [[a]] processor ~~within the data processing device,~~

wherein the step of cyclically apportioning a current flow switches ~~that is periodically or aperiodically switched~~ between multiple different nonzero substantially constant current levels, the switching being one from among periodic and aperiodic, and the switching being such that the drawn current varies independently of the instantaneous power demand of the processor.

21. (Currently Amended) The method of claim 20 wherein ~~further including~~ the step of ~~utilizing the drawn current to generate~~ cyclically apportioning a current flow to the processor and the charge storage device switches, ~~that is~~ periodically or aperiodically, ~~switched~~ between two different nonzero substantially constant current levels.

22. (Canceled)

23. (Currently Amended) The method of claim 21 wherein ~~further including~~ the step of cyclically apportioning a current flow includes determining the interval between switching according to an average power demand of the processor.

24. (Currently Amended) The method of claim 20 wherein the step of cyclically apportioning a substantially constant current flow utilizes a first current source, and further including ~~the steps of~~:

utilizing a second current source to provide a superposed current that varies on a random or pseudorandom basis and

delivering the combined current of the first and second current sources to the processor and the charge storage device.

25. (Previously Presented) The method of any one of the claims 20, 21, 23, and 24 further including the step of maintaining a supply voltage to the processor between an upper voltage limit and a lower voltage limit.

26. (Currently Amended) The method of claim 25 wherein ~~further including~~ the step of cyclically apportioning a substantially constant current flow switches the ~~switching a~~ current source between a first, higher current level and a second, lower, current level, when the supply voltage to the processor respectively reaches the lower voltage limit and the higher voltage limit.

27. (Currently Amended) The method of claim 26 wherein the step of cyclically apportioning a substantially constant current flow further includes ~~including~~ the steps of:

determining a time period taken for the processor supply voltage to reach a lower voltage limit from an upper voltage limit, or vice versa, and

varying the first current level and/or the second current level of the current source if the time period falls outside predetermined limits.

28. (Currently Amended) The method of claim 27 wherein said step of varying further includes ~~including the step of~~ raising the first current level if the time period for reaching the lower voltage limit falls below a first predetermined threshold.

29. (Currently Amended) The method of claim 27 wherein said step of varying further includes ~~including the step of~~ reducing the first current level if the time period for reaching the lower voltage limit exceeds a second predetermined threshold.

30. (Currently Amended) The method of claim 27 wherein said step of varying further includes ~~including the step of~~ reducing the second current level of the time period for reaching the upper voltage limit falls below a first predetermined threshold.

31. (Currently Amended) The method of claim 27 wherein said step of varying further includes ~~including the step of~~ raising the second current level if the time period for reaching the upper voltage limit exceeds a second predetermined threshold.

32. (Currently Amended) The method of claim 26 further including the step of temporarily inhibiting the current switching if the supply voltage to the processor fails to move towards the ~~desired~~ upper voltage limit or the lower voltage limit.

33. (Original) The method of claim 20 further including the step of controlling the frequency of operation of the processor as a function of the supply voltage to the processor.

34-35. (Canceled)

36. (Currently Amended) The method of claim 28 wherein said step of varying further includes ~~including the step of~~ reducing the first current level if the time

period for reaching the lower voltage limit exceeds a second predetermined threshold.